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Demonstration of nonvolatile multilevel memory in ambipolar carbon nanotube thin-film transistors

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Multilevel memories have attracted significant interest because of their larger memory density per unit cell. Here, we investigated multilevel operation with ambipolar carbon nanotube thin-film transistors. Three distinct conduction states and a direct change between any of them were demonstrated by selecting appropriate values for the magnitude and duration of each program/erase voltage pulse. A low operation voltage of 5 V and a short duration of 1 s were obtained by utilizing a bilayer Al_2O_3-epoxy dielectric to enhance the gate modulation efficiency. A tradeoff exists between low-voltage operation and fast switching for a given device. © 2015 The Japan Society of Applied Physics

Carbon nanotubes (CNTs) have been widely studied because of their superior electrical properties, such as a high current density[1)] and good carrier mobility.[2)] Efforts have been made to fabricate field-effect transistors (FETs) and integrated circuits based on individual CNTs[3)] and CNT networks[4)] to develop their applications in future electronics. A demo CNT computer has recently been reported,[5)] which further demonstrates the potential application of CNTs in next-generation electronics. One of the primary components in electronic systems with a complete data processing functionality is the memory unit. A variety of binary data storage devices have been reported using CNTs as small-scale electrodes in resistive or phase change memory,[6,7)] as charge storage nodes in floating gate transistors or metal–insulator–semiconductor capacitors,[8–10)] and as active channels in hysteretic FETs.[11,12)] Among these reported devices, hysteretic CNT-FETs can be integrated as memory elements in CNT-based electronic systems because FETs are the primary constituent parts of an electronic circuit. There have been several efforts to demonstrate CNT-FET-based memory devices. An individual CNT-based FET memory device was reported with a high mobility of 9000 $cm^2/(V{\cdot}s)$, which enables the storage and detection of a single or few electrons at a temperature of up to 100 K.[2)] The write/erase speed of CNT-FET memory devices was improved to 100 ns using a high-k gate dielectric,[13)] while good retention performance (14 d)[14)] was achieved with a two-stage hydrogen and air annealing process. Additionally, a flexible memory device based on a CNT-FET was realized using a transfer method.[12)] These reports demonstrated the potential of CNT-FETs in memory devices for electronic systems.

Several research groups have focused on the multilevel operation of CNT-FET memory devices,[15–17)] because the multilevel data storage capability can increase the memory density per unit cell. In these studies, multilevel storage states were achieved by introducing a floating gate in the top-gate FET configuration, or using the intrinsic hysteresis effect originating from the polarization of molecules in a global back-gate FET configuration. Because of inherent problems in the device structure, the devices suffer from a large operating voltage, a low program/erase speed, the need for multiple program pulses, or a non-zero gate bias (V_{GS}) for read out. The exposure of a CNT channel to air in the back-gate configuration could make the device vulnerable to the ambient environment. Furthermore, the ability to program/erase the device between any of the memory states has not been demonstrated.

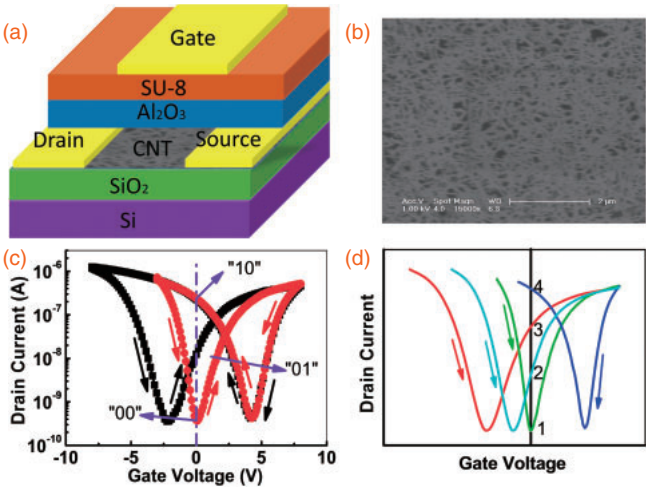

Fig. 1. (a) Schematic of the top-gate ambipolar CNT-TFT. (b) Scanning electron microscopy image of CNT film. (c) Multilevel transfer characteristics of an ambipolar CNT-FET gate voltage between −3 and 8 V (red) and between −8 and 8 V (black). The drain–source bias was 0.5 V. (d) Schematic illustration of the full potential.

Here, we achieved three distinct conductance levels based on ambipolar CNT-TFTs by selecting appropriate values for the magnitude and duration of each program/erase voltage pulse. The device can be programmed/erased between any of the three states. The maximum program voltage was reduced to 5 V because of the high gate modulation efficiency of the channel. The improvement of gate modulation efficiency was realized by using high-capacitance bilayer Al_2O_3-epoxy as a dielectric.[18)] The maximum program duration was 1 s to erase the device to the "00" state.

The device structure is shown schematically in Fig. 1(a). The CNT random network was formed on a SiO_2/Si substrate functionalized with 3-aminopropyltriethoxysilane. The CNTs had a semiconductor purity of 99%. Au was deposited by electron-beam evaporation to form source and drain contacts. An Al_2O_3 thin film of 35 nm thickness was em-

ployed as the gate dielectric and deposited by atomic layer deposition. An additional 10 nm layer of cross-linked epoxy (SU-8 2002) was spin-coated on top.

It was suggested that the top-gate configuration had better electrostatic coupling with the cylindrical CNT channel. Together with a high-k dielectric, low-voltage transistor operation can be achieved.[18,19] Additionally, Al_2O_3 can induce substantial hysteresis in an initially hysteresis-free device[20] while the additional epoxy layer can make the dielectric robust, smooth, and pinhole-free with low leakage.[18] We therefore constructed our TFT of this structure.

Figure 1(c) shows the transfer characteristics of the as-fabricated CNT-TFT measured at a drain–source bias (V_{DS}) of 0.5 V. Two gate sweep ranges, namely, −3 to 8 V (red) and −8 to 8 V (black), were used. An ambipolar behavior with hystereses of 4.24 and 6.56 V for the two sweeps was achieved. Here, hysteresis is defined by the difference between the minimum conduction voltages of forward and reverse sweeps. It increases when the gate voltage sweeping range increases, as observed by others.[12,14,21,22] Because the CNT channel is isolated from air, adsorbed molecules (such as oxygen and water molecules) are not responsible for the observed hysteresis. We ascribe the hysteresis to charge injection from the CNT to charge traps in the high-k dielectric[13] and at the CNT/dielectric interface.[23] Three conduction levels were observed at zero gate voltage after gate voltage sweeps of 8, −8, and −3 V, indicating that multilevel data storage could be achieved. The voltage used here is not the same as the program/erase voltage in memory operation because the magnitude of the hysteresis also depends on the sweeping rate[24] or the gate voltage pulse duration. We schematically illustrated the full potential of this type of device in Fig. 1(d). Because the conductance at $V_{GS} = 0$ V can be continuously changed by adjusting the negative gate stress, it can show four or more memory states limited by the ratio of the maximum conductance to the minimum conductance.

To demonstrate the multilevel memory operation, program/read/erase cycles were performed, as shown in Fig. 2. W1 and W2 are the gate voltage pulses used to program the device, and E0 and E1 are those used to erase the device. A short, positive gate voltage pulse can program the device from a relatively low conduction state to a relatively high conduction state, whereas, a negative gate voltage pulse can erase the device by reversing the conduction state. Three conduction states can be distinctly read out at $V_{GS} = 0$ V and each state can be directly changed to any other state with a single pulse. Note that four different gate voltage pulses (W1, W2, E0, and E1) are needed to obtain the three conduction states, because the gate pulse to write the device to the "01" state is dependent on whether the device is in the "00" or "10" state. This difference means that the data should be read out before transforming the device to the "01" state. Furthermore, because W1 and E1 correlate to E0 and W2, respectively, it is difficult to find the appropriate gate voltage pulse to achieve a reproducible direct change between the different states.

We overcome this drawback by measuring the electrical states of the device for many given combinations of gate stresses and adjusting every gate stress. Finally, we picked the combination of W1 = 1.6 V, 0.01 s; W2 = 5 V, 0.1 s; E0 = −4 V, 1 s; and E1 = −2.3 V, 1 s for the device shown

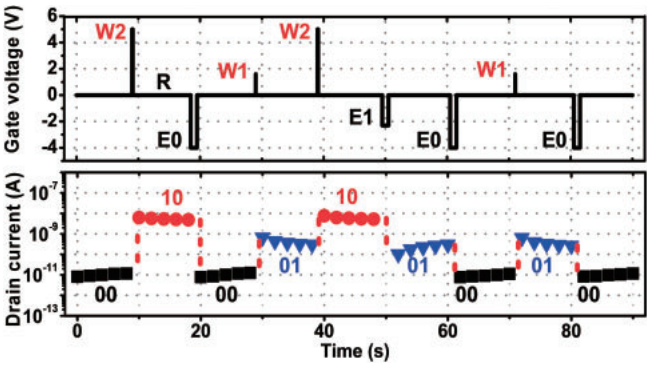

Fig. 2. Three conduction states of the multilevel memory cell measured at zero gate bias and $V_{DS} = 0.01$ V. W1 and W2 are the corresponding program gate voltage pulses and E0 and E1 are the erase gate voltage pulses.

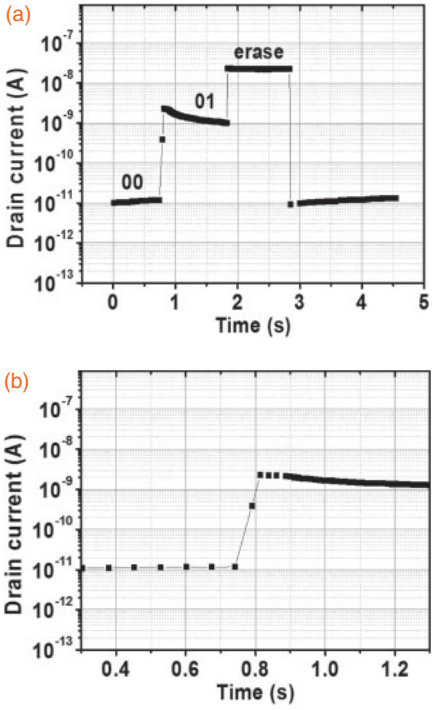

Fig. 3. Response rising time of drain current when gate voltage pulse is applied. (a) Response of drain current when a writing gate pulse (1.6 V, 0.01 s) and an erasing gate pulse (−4 V, 1 s) are applied. (b) Zoom on the response of the drain current when a writing gate pulse is applied.

in Fig. 2 to achieve a reproducible direct change between the different states. In this way, we demonstrated that a direct change between any of the states is possible in CNT-TFT-based multilevel memory devices. Operating speed is a key performance indicator of a memory device. In our device, the erasing and writing operation is carried out with a gate voltage pulse of appropriate magnitude and duration. The memory states are recorded before and after the voltage pulse. However, it is still important to investigate the response rising time of I_{DS} current when the gate voltage pulse is applied. Figure 3 shows the response of drain current when a writing gate pulse (1.6 V, 0.01 s) and an erasing gate pulse (−4 V, 1 s) are applied. The drain current of around 2×10^{-9} A corresponds to the 01 state, while the drain current larger than 10^{-8} A corresponds to the erase current. As can be seen from Fig. 3(b), the response rising time of I_{DS} current is 0.07 s.

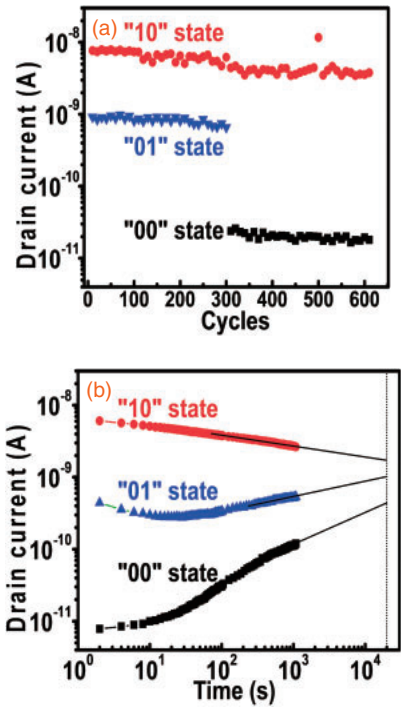

Fig. 4. Stability of the device measured at zero gate bias and $V_{DS} = 0.01$ V. (a) Endurance and (b) retention properties of the three states.

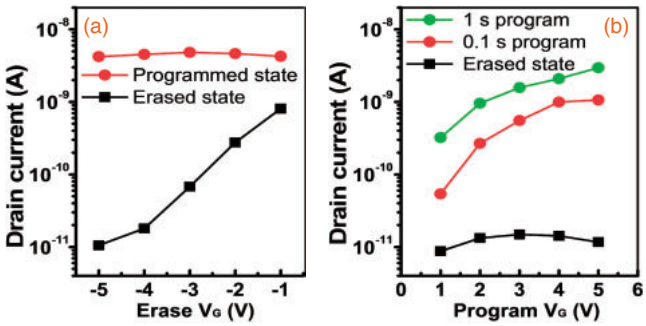

Fig. 5. Drain current as a function of magnitudes of (a) erase and (b) programmed gate pulses. The duration of erasing is 1 s and those of programming are 0.1 s (red) and 1 s (green).

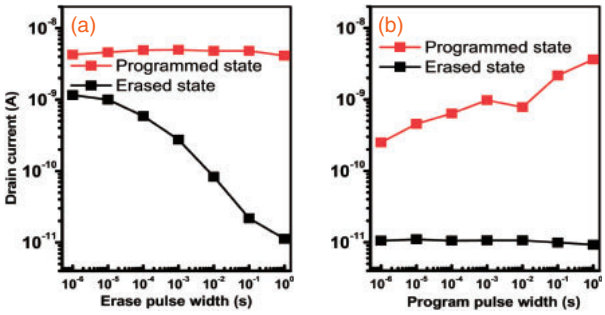

Fig. 6. Current change as a function of the durations of (a) erase gate pulse and (b) program gate pulse. In both cases, the magnitudes are −4 V for erasing and 5 V for programming.

We further studied the reliability of the multilevel memory. Figure 4(a) shows the endurance characteristics of the device over 600 write/read/erase cycles. No significant degradation was observed, whereas the drain current of the "10" state was slightly smaller for the latter 300 cycles than for the former 300 cycles. This is because the latter 300 cycles were performed between the "10" state and the "00" state with the gate stresses W2 and E0, respectively, whereas the former 300 cycles were performed between the "10" state and the "01" state with the gate stresses W2 and E1, respectively. The same gate stress, W2 (5 V, 0.1 s), should induce the same amount of negative charge to be trapped. However, there are less negative trapped charges in the "00" state than in the "01" state. Thus, the negative charge amount after W2 is not the same. This phenomenon means that the conductance after a given gate voltage pulse depends on the previous charge status of the device when the voltage pulse magnitude and/or duration is not sufficiently large to reach a saturated state. It is well consistent with the previous observation that the choice of the program/erase voltage pulse for the "01" state correlates to the previous status of the device.

The volatility of the device was evaluated by measuring the retention time as plotted in Fig. 4(b). A slight decay of the three states over a period of 1000 s was observed. This decay is ascribed to the dissipation of injected charges near the CNTs.[23] As extrapolated in Fig. 4(b), the states can be maintained for 2.5×10^4 s. The retention performance was not as good as those of other similar multilevel or binary memory devices because the gate stress duration used here for the retention test was much shorter than that used in other studies.[11,12]

As the conduction state directly depends on the gate stress, we measured the dependence of drain current on the magnitude of the gate voltage pulse as shown in Fig. 5. The device was reset with the same gate voltage pulse before measuring each data point to start with a common initial status as the standard reference. Each data point was read out at a gate bias of 0 V and $V_{DS} = 0.01$ V. Figure 5(a) shows that as the magnitude of the negative erase pulse increases, the drain current continuously decreases, which indicates that more charges accumulate in the vicinity of the CNTs. The decrease in drain current also indicates that the FET channel shows p-type conduction after a negative voltage pulse because the negative gate voltage shifts the threshold voltage towards negative values. Figure 5(b) shows that the drain current increases as the positive program voltage increases, because the threshold voltage shifts more positively. When the program voltage is larger than 5 V, the current increase is negligible because it already saturates. The increase also indicates that the channel conducts holes at $V_{GS} = 0$ V because the minimum conduction voltage is positive after positive gate stress.

Combining these two observations, we propose that the FET always works in the hole conduction mode at zero gate bias after a program/erase voltage pulse despite the ambipolar transfer characteristics.

The possible operation frequency was characterized by measuring the dependence of drain current on pulse duration. To have a common reference, a reset operation was carried out before measuring each data point. As the negative erase voltage pulse duration increased from 10^{-4} to 1 s, the drain current of the erased state decreased 100-fold, as shown in Fig. 6(a). This is because there was sufficient time for trapped charges to accumulate. A similar behavior was observed for the programmed drain current as shown in Fig. 6(b). By combining the results shown in Figs. 5 and 6, it can be seen

that the drain current depends on both the magnitude and duration of gate stress. For a given device, the magnitude of program/erase voltage should be increased for faster switching, and vice versa. For example, in Fig. 5(b), when the duration is increased to 1 s (green), only 2 V is sufficient for programming the drain current to 1 nA rather than 4 V (red). There is a tradeoff between low-voltage operation and fast switching for a given device.

In summary, we have demonstrated multilevel data storage using ambipolar CNT-TFTs. Three clearly distinguishable conduction states were achieved and could be directly interchanged between each other by selecting appropriate values for the magnitude and duration of each program/erase voltage pulse. It was suggested that a tradeoff existed between low-voltage operation and fast switching for a given device through a detailed study of the dependence of the drain current on the magnitude and duration of the gate voltage stress.

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